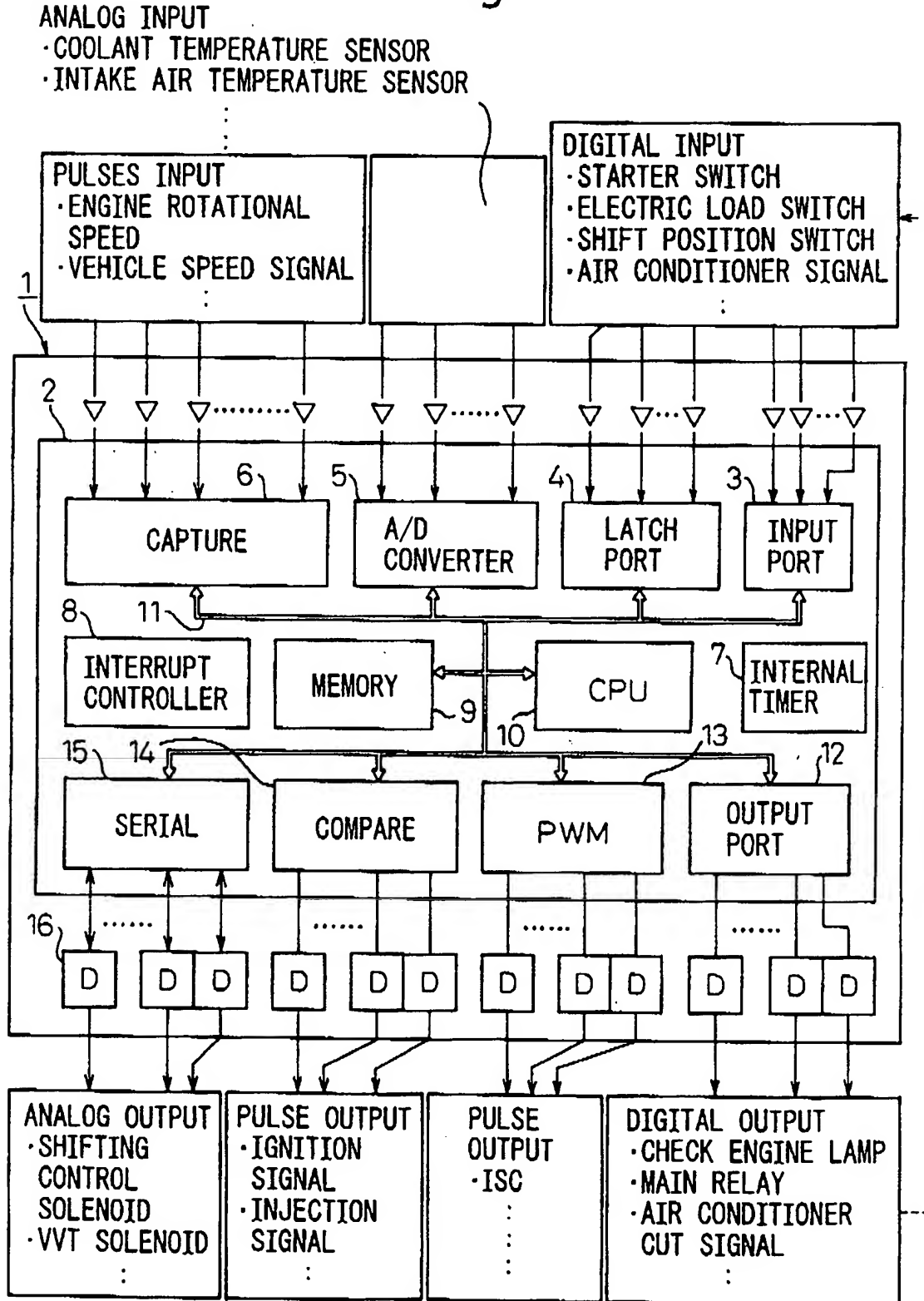


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Fig.1



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Fig.2

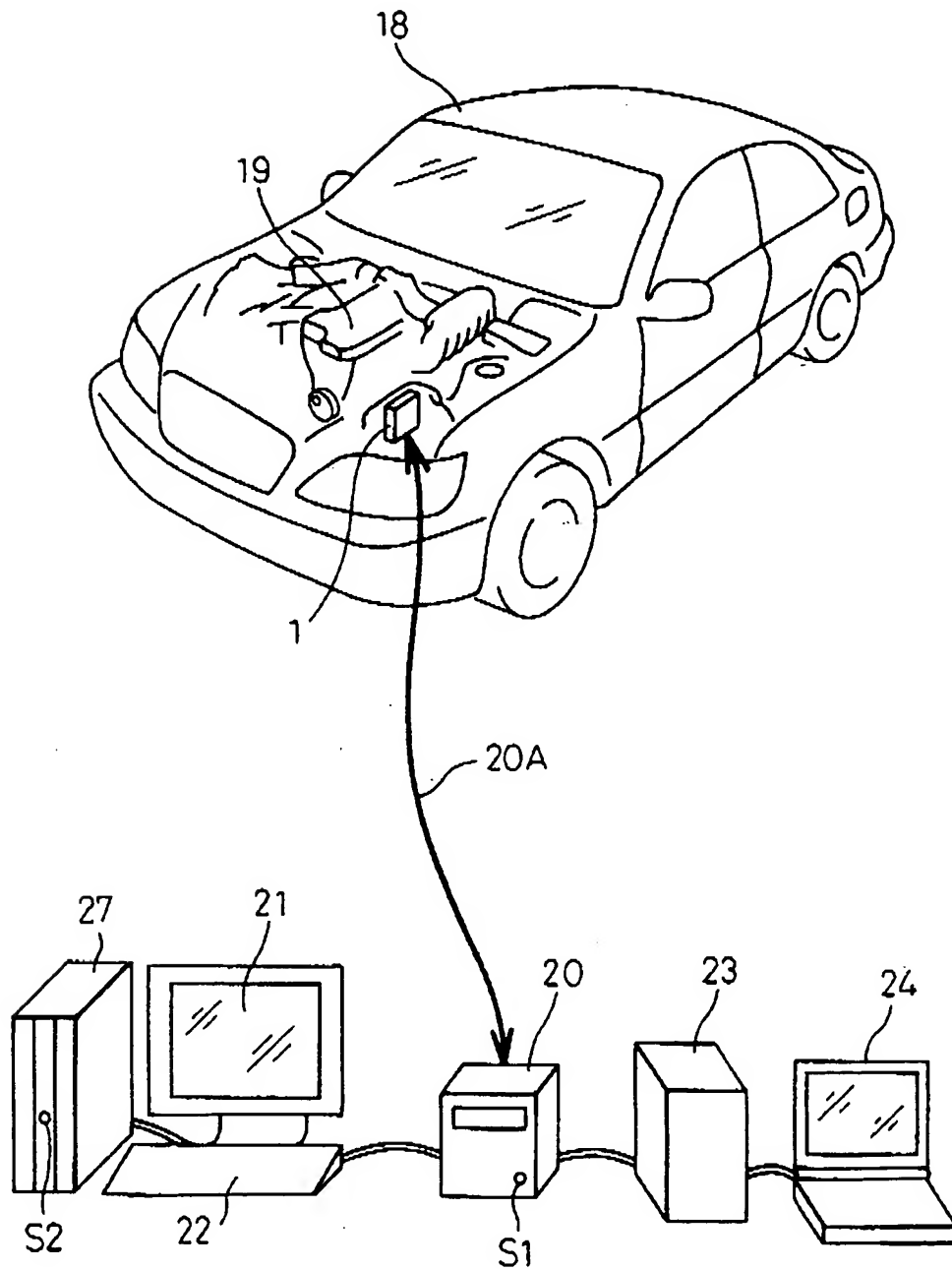
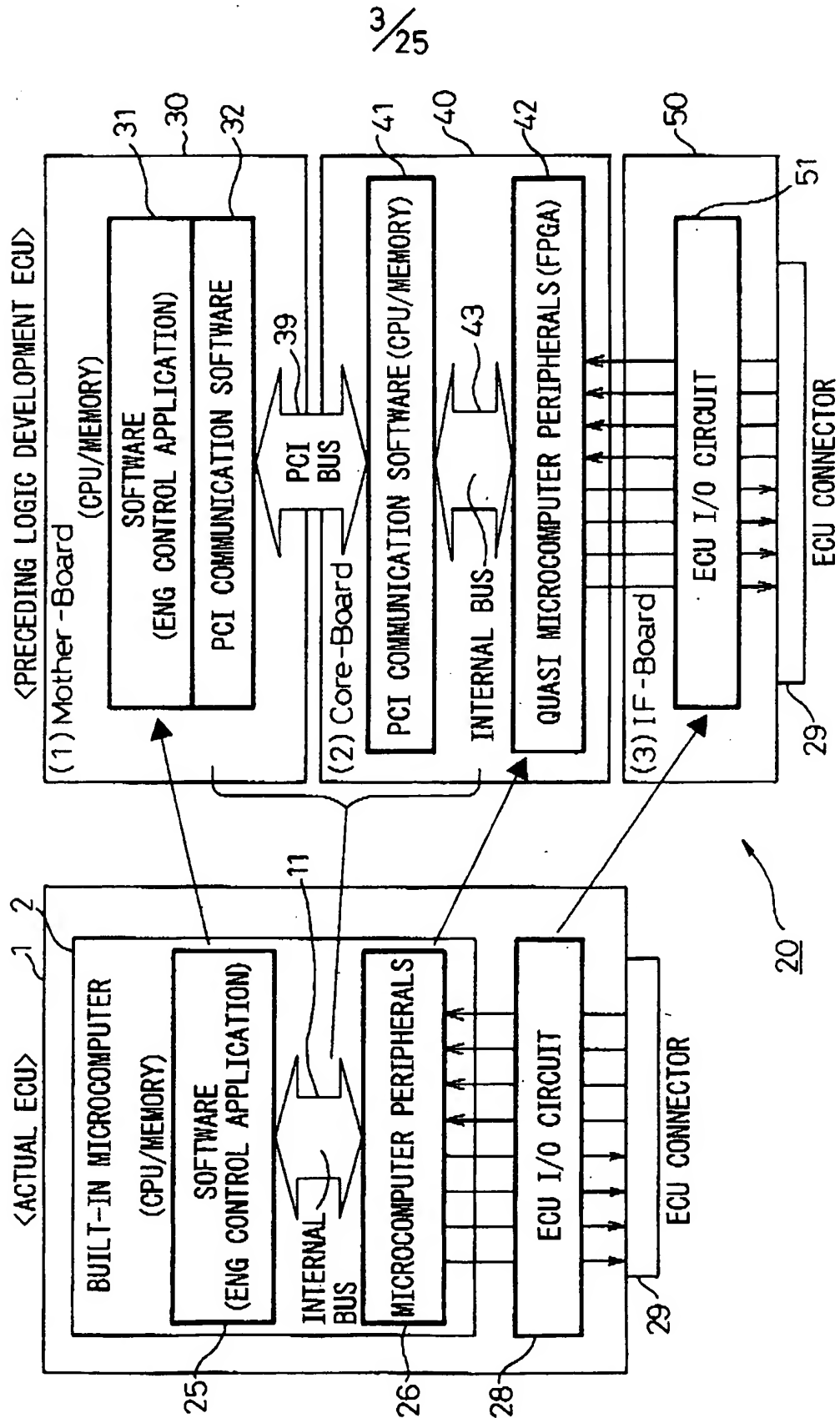
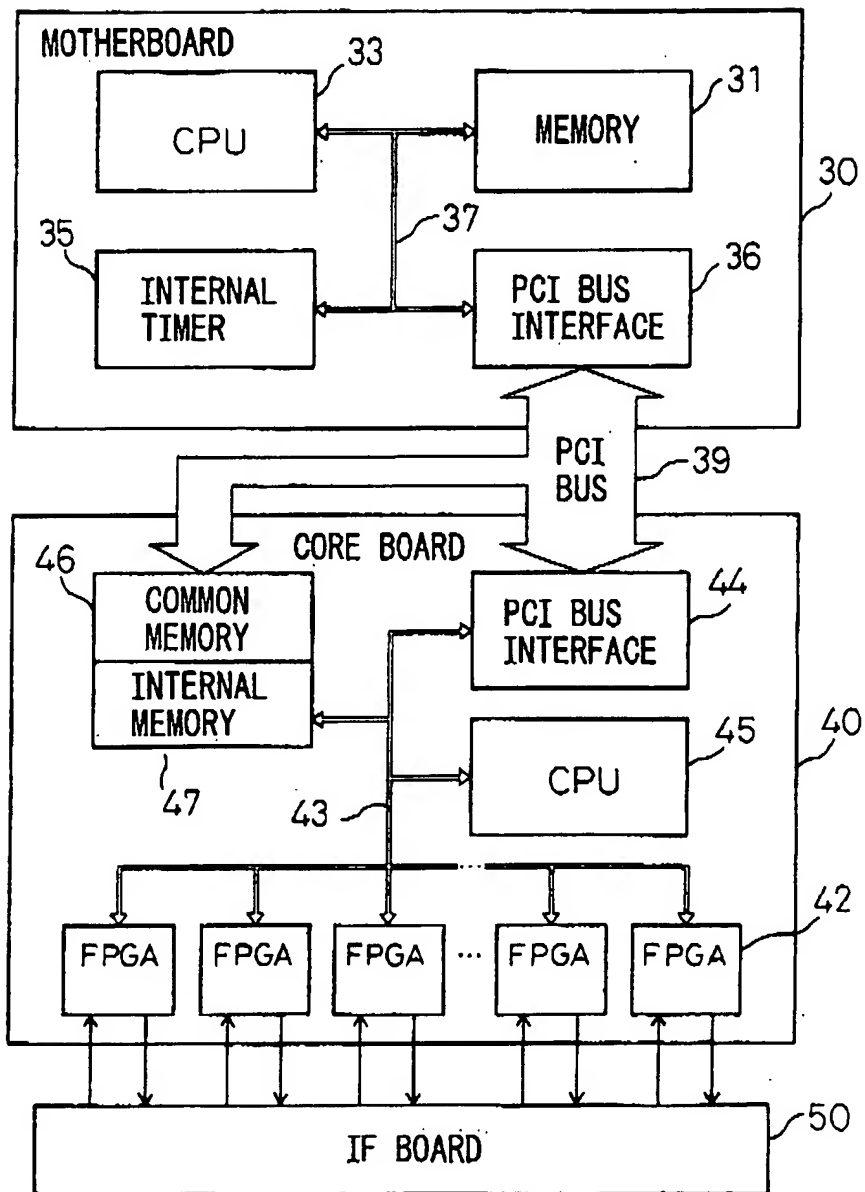


Fig.3



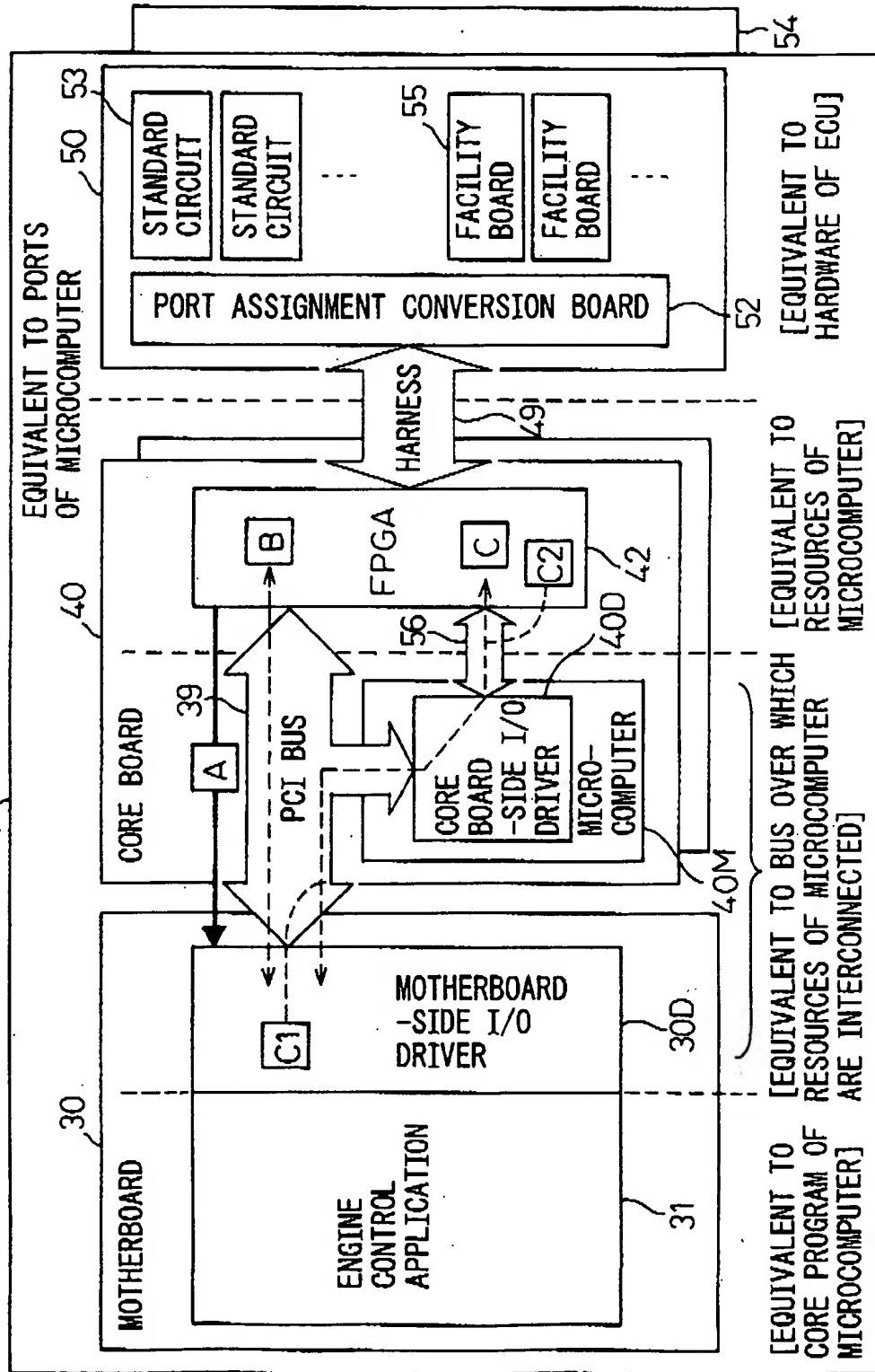
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Fig.4



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Fig.5



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Fig.6

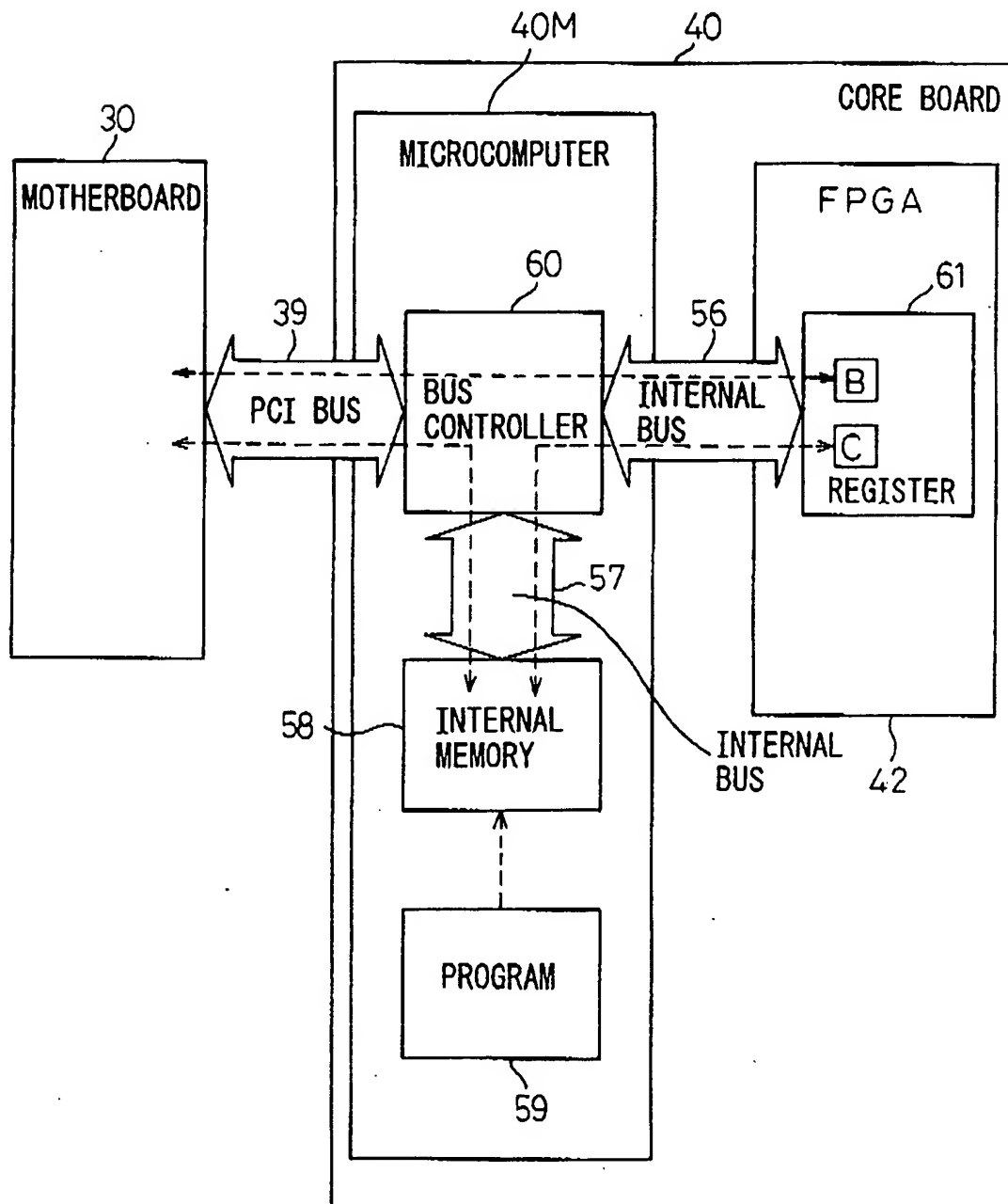
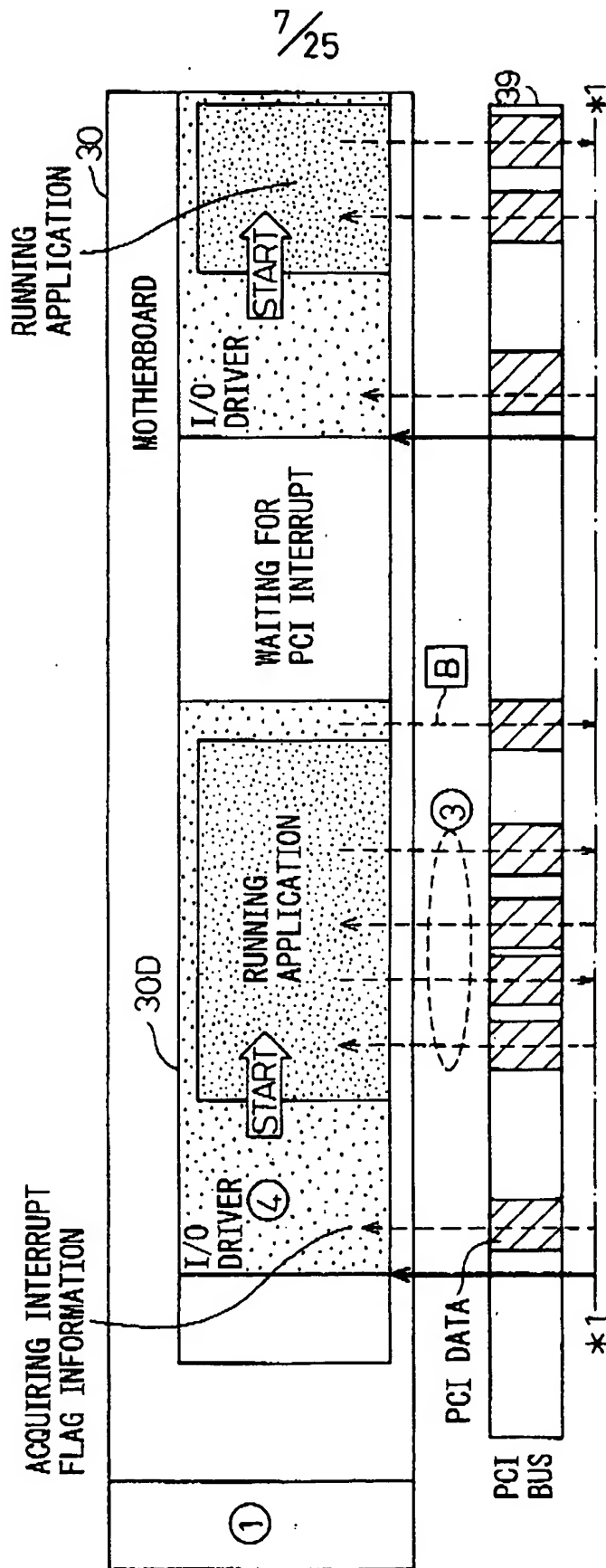
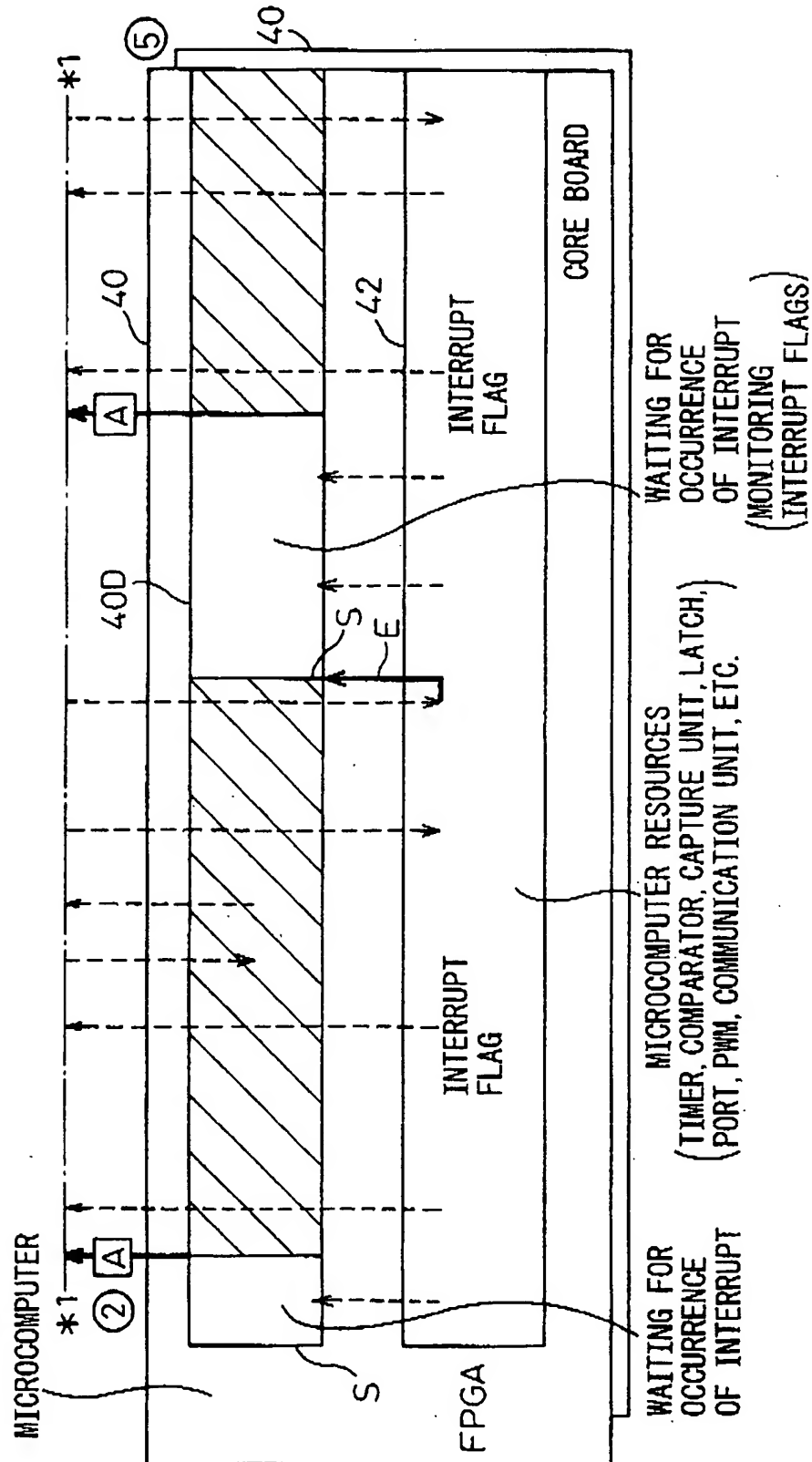


Fig. 7A



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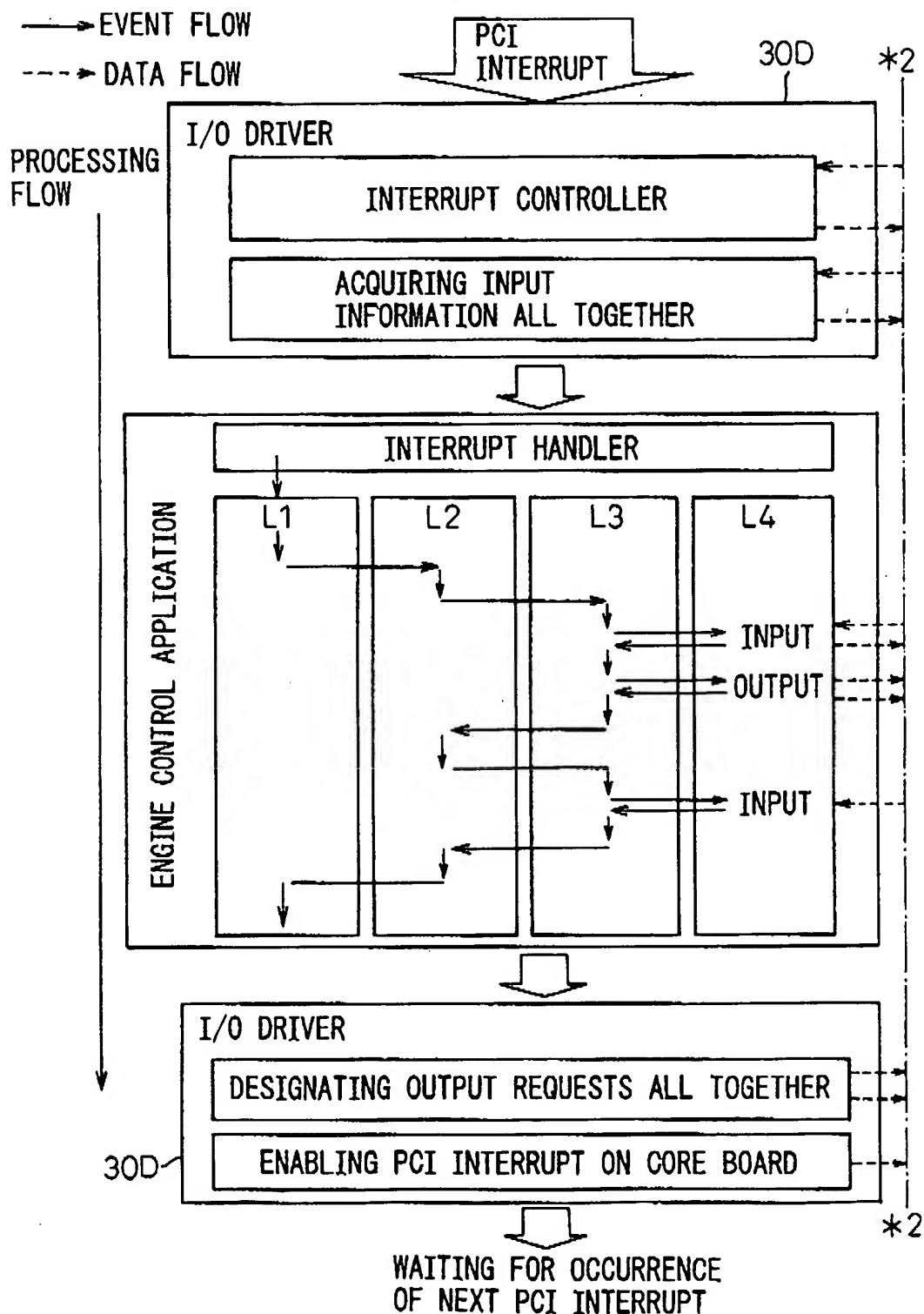
Fig.7B





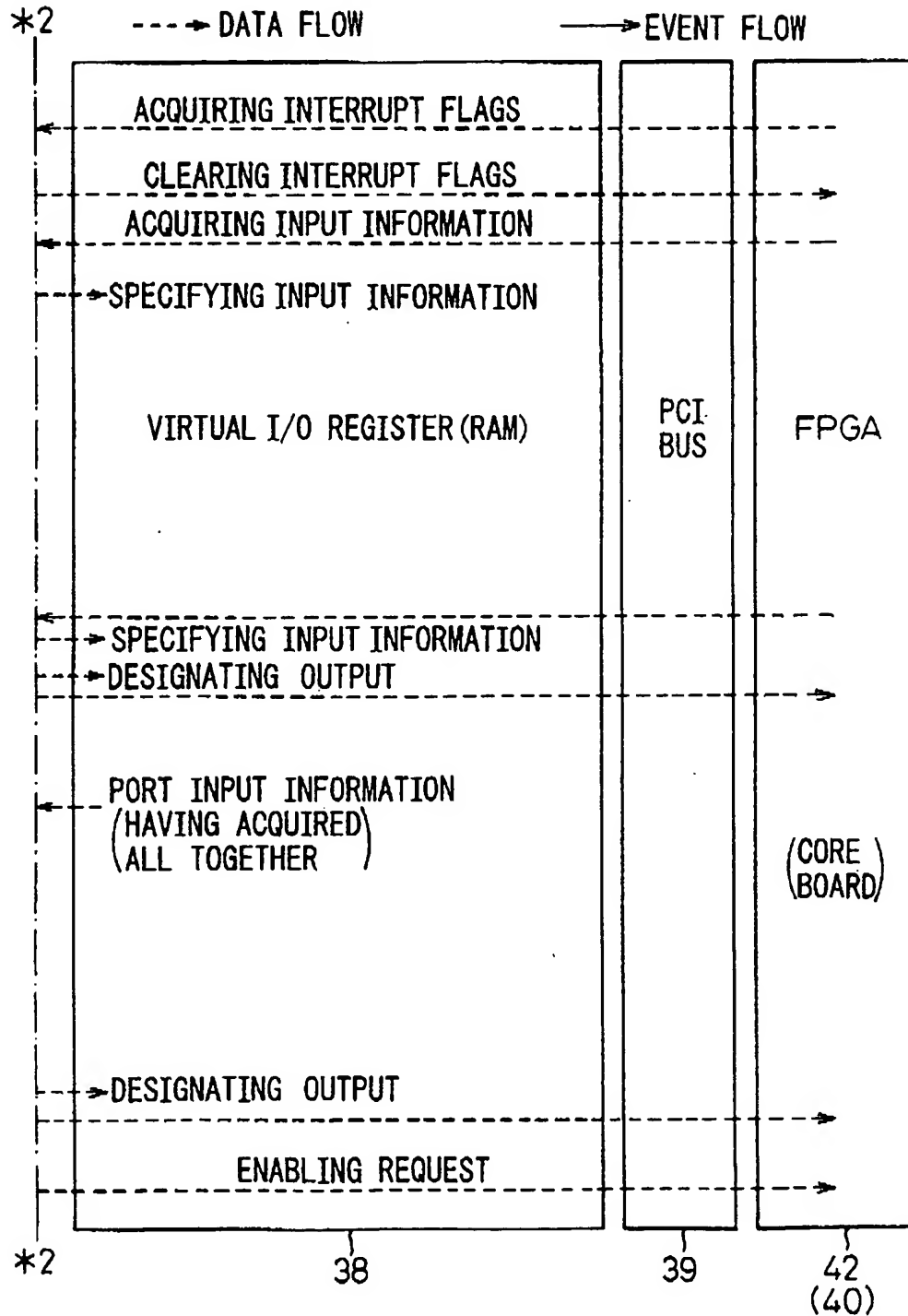
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Fig.8A



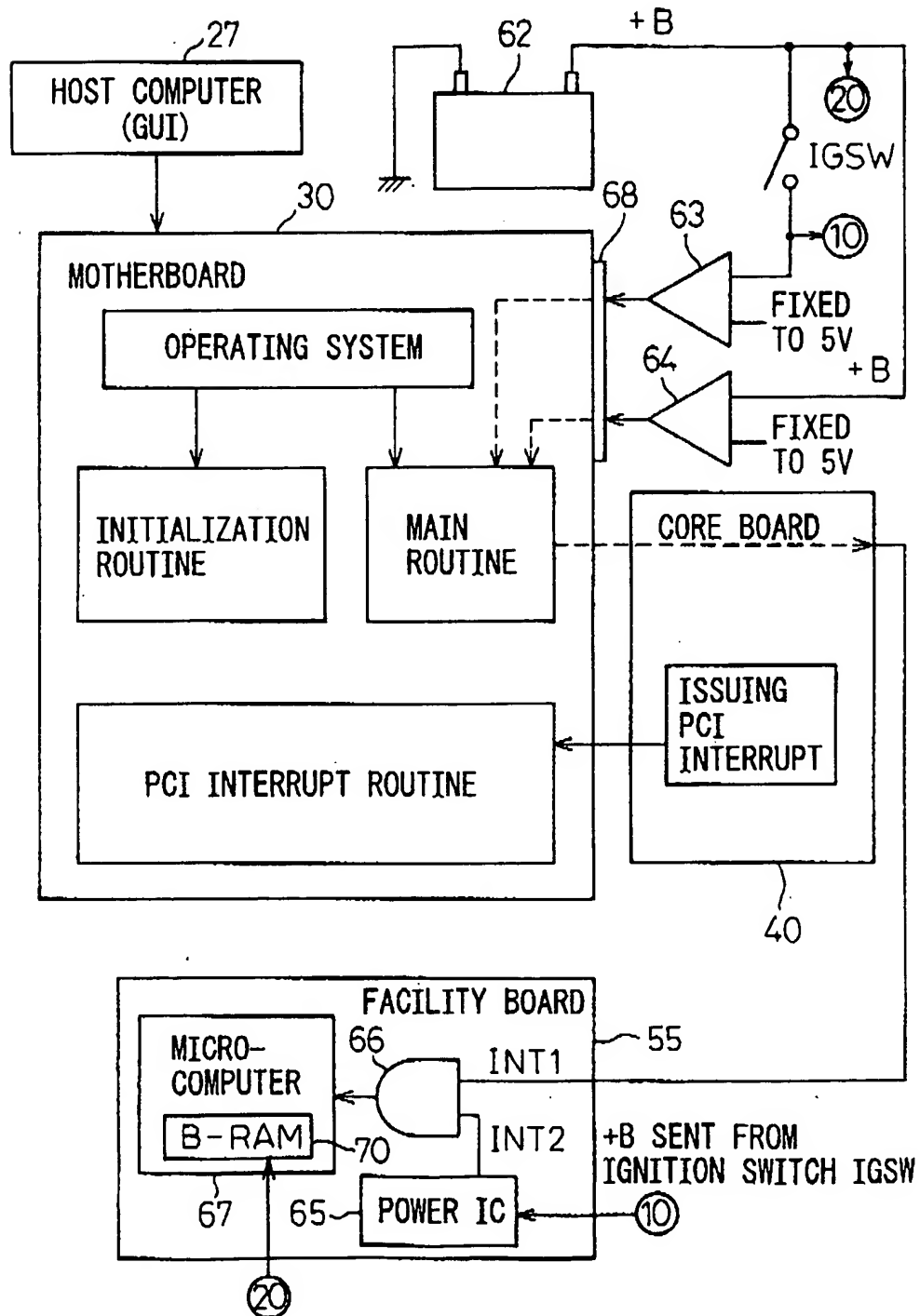
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Fig.8B



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Fig.9



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Fig.10A

	MOTHERBOARD	CORE BOARD	FACILITY BOARD
1	AN ENGINEER TURNS ON THE POWER SUPPLY OF THE SYSTEM.	DITTO	THE POWER SUPPLY IS OFF.
2	SOFTWARE IS DOWNLOADED FROM THE HOST COMPUTER, AND THE MOTHERBOARD IS ACTIVATED.	DITTO	
3	INITIAL VALUES TO WHICH PORTS ARE SET ARE DETERMINED. (X1) (1) THE COMPARETOR IS SET TO AN IMMEDIATE OUTPUT MODE. (2) THE PHM IS SET TO A 0% OUTPUT MODE. (3) THE SIGNAL INIT1 IS DRIVEN LOW. (4) THE MAIN ROUTINE IS SET TO STATE 1.	PCI INTERRUPTS ARE LOCKED.	
4	ACTION OF STATE 1 (1) A WAIT STATE IS MAINTAINED UNTIL THE SWITCH IGSW IS TURNED ON.		
5	(2) WHETHER THE SWITCH IGSW IS TURNED ON IS DETECTED. (3) THE MAIN ROUTINE IS SET TO STATE 2.		THE POWER SUPPLY IS TURNED ON.

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Fig.10B

6	<p>ACTION OF STATE 2</p> <p>(1) THE CONTENTS OF A MEMORY ARE RESTORED  (WHEN THE BATTERY IS REMOVED.)  DATA IS INITIALIZED.</p> <p>(2) DATA IN AN EEPROM IS RESTORED.</p> <p>(3) THE MAIN ROUTINE IS SET TO STATE 3.</p>		POWER-ON RESET TIME (POWER IC)
7	<p>ACTION OF STATE 3</p> <p>(1) A WAIT STATE FOR WAITING UNTIL A POWER-ON RESET TIME ELAPSES IS MAINTAINED.</p>		
8	<p>(2) THE POWER-ON RESET TIME ELAPSES.</p>		THE SIGNAL INIT2 IS DRIVEN HIGH.
9	<p>(3) THE SIGNAL INIT1 IS DRIVEN HIGH.</p> <p>(4) FACILITIES OTHER THAN THE COMMUNICATION FACILITY ARE INITIALIZED.</p> <p>(5) THE MAIN ROUTINE IS SET TO STATE 4.</p>		THE SIGNAL INIT1 IS DRIVEN HIGH. BOTH THE SIGNALS INIT1 AND INIT2 ARE HIGH. THE RESET STATE IS CANCELED.
10	<p>ACTION OF STATE 4</p> <p>(1) A WAIT STATE IS MAINTAINED UNTIL THE INITIALIZATION TIME REQUIRED FOR THE FACILITY BOARD ELAPSES.</p>		INITIALIZATION
11	<p>(2) THE INITIALIZATION TIME REQUIRED FOR THE FACILITY BOARD ELAPSES.</p> <p>(3) COMMUNICATION OF INITIALIZATION DATA TO THE FACILITY BOARD IS STARTED.</p> <p>(4) THE MAIN ROUTINE IS SET TO STATE 5.</p>	DMA COMMUNICATION	THE MAIN PROCESS IS DOWNLOADED.
12			

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Fig.11A

	MOTHERBOARD	CORE BOARD	FACILITY BOARD
12	ACTION OF STATE 5 (1) A WAIT STATE IS MAINTAINED UNTIL COMMUNICATION OF INITIALIZATION DATA TO THE FACILITY BOARD IS COMPLETED.		DATA IS RECEIVED, AND TRANSMISSION DATA IS PRODUCED.
13	(2) SENSING COMPLETION ← ×IF A TIMEOUT OCCURS WITHOUT COMPLETION, THE MAIN ROUTINE IS RETURNED TO STATE 4.		THE TRANSMISSION DATA IS TRANSMITTED.
14	ACTION OF STATE 6 (1) INITIALIZATION IS COMPLETED.		
15	(2) A REQUEST FOR UNLOCKING PCI INTERRUPTS IS ISSUED TO THE CORE BOARD. (3) THE MAIN ROUTINE IS SET TO STATE 7.	ALL THE INTERRUPT FLAGS ARE CLEARED. PCI INTERRUPTS ARE UNLOCKED.	

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Fig.11B

16	ACTION OF STATE 7 (1) A WAIT STATE IS MAINTAINED UNTIL THE SWITCH IGSW IS TURNED OFF.	PCI INTERRUPT HANDLING	COMMUNICATION OF A PCI INTERRUPT REQUEST IS STARTED.	
17	(2) IT IS DETECTED WHETHER THE SWITCH IGSW IS TURNED OFF. (3) THE MAIN ROUTINE IS SET TO STATE 8.			THE POWER SUPPLY IS TURNED OFF.
18	ACTION OF STATE 8 (1) A REQUEST FOR LOCKING PCI INTERRUPTS IS ISSUED.		PCI INTERRUPTS ARE LOCKED.	
19	(2) THE DATA IN THE MEMORY AND EEPROM IS PRESERVED.		PCI INTERRUPTS ARE DISABLED.	
20	(3) THE PORTS ARE SET TO INITIAL VALUES. SAME AS (※1) (AFTER INITIALIZATION IS COMPLETED, ) (THE MAIN ROUTINE IS SET TO STATE 1.)			

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Fig.12A

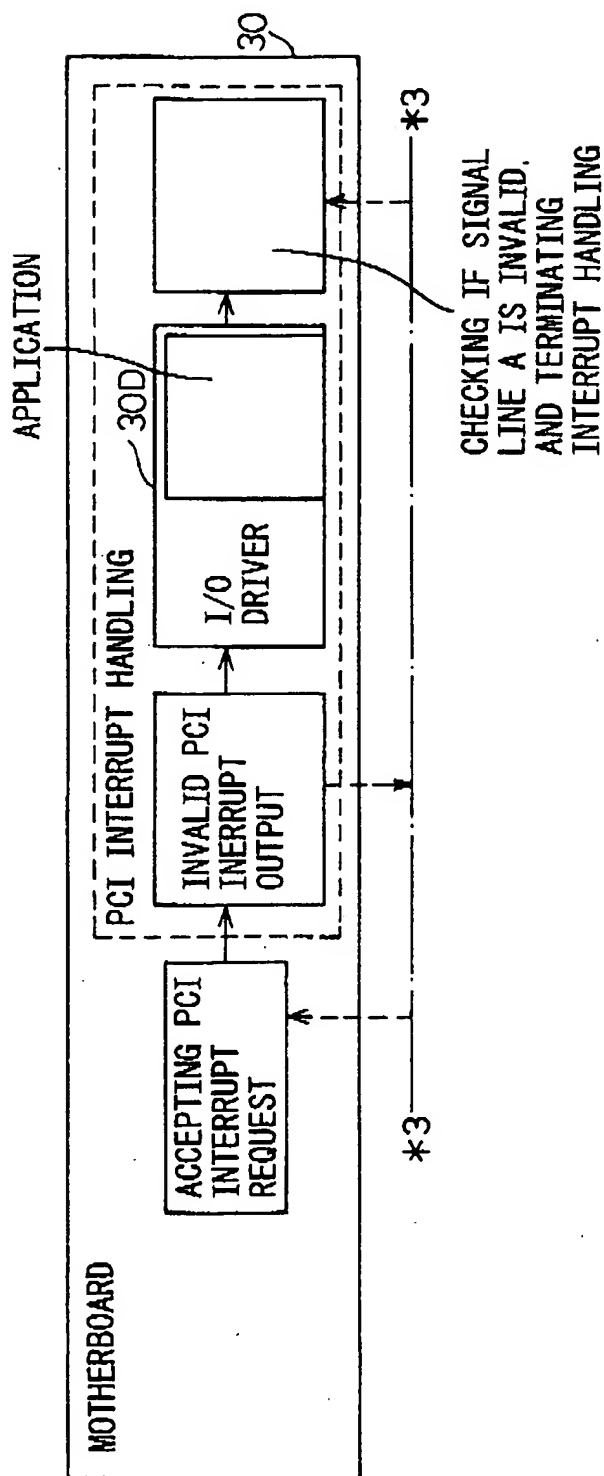




Fig.12B

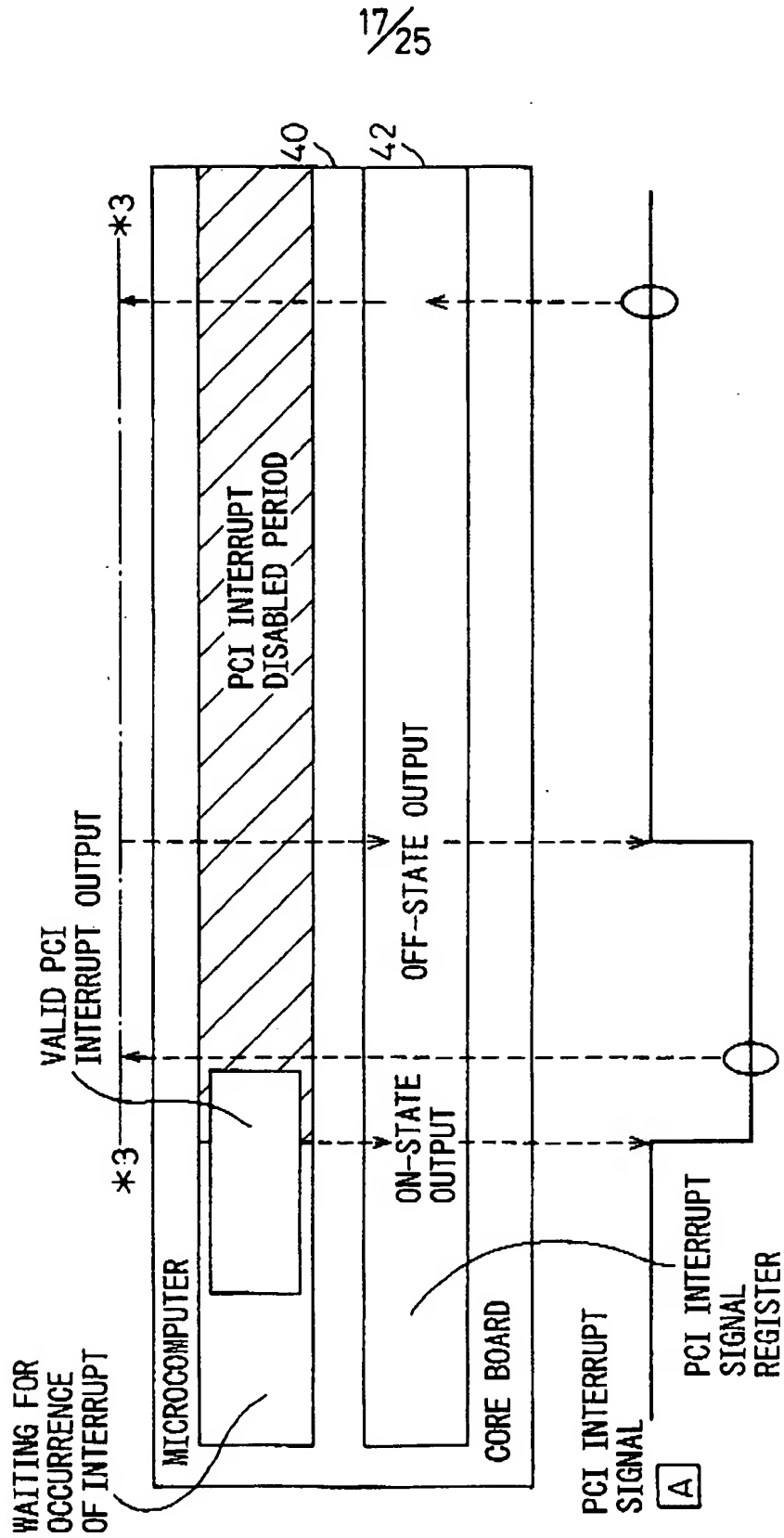


Fig.13A

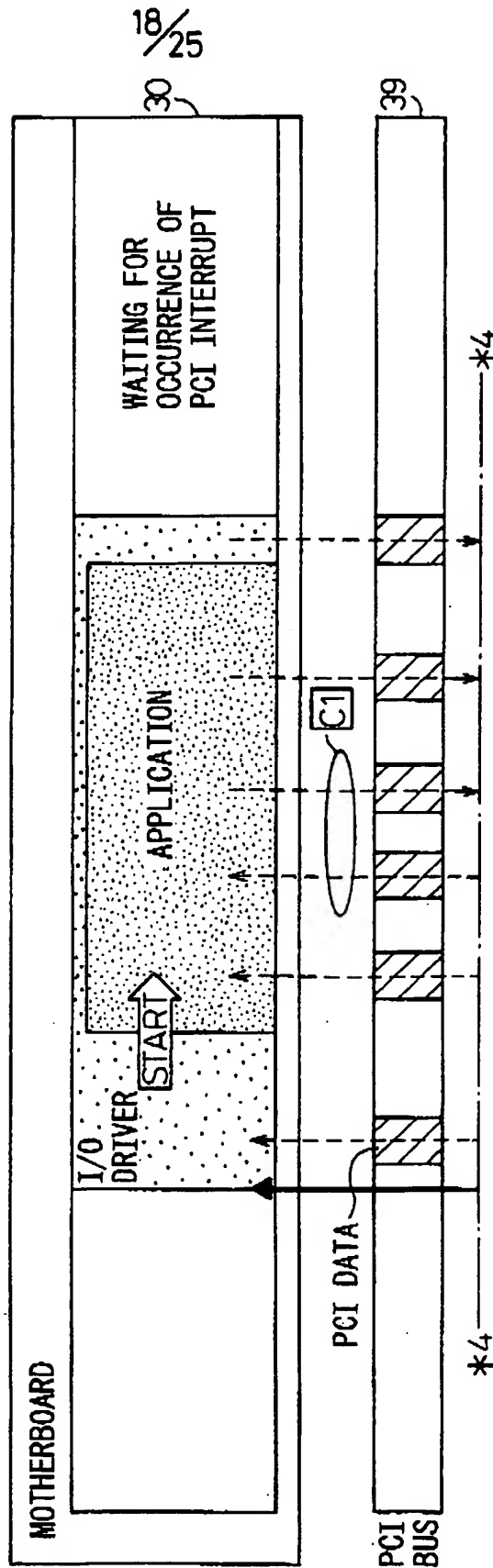
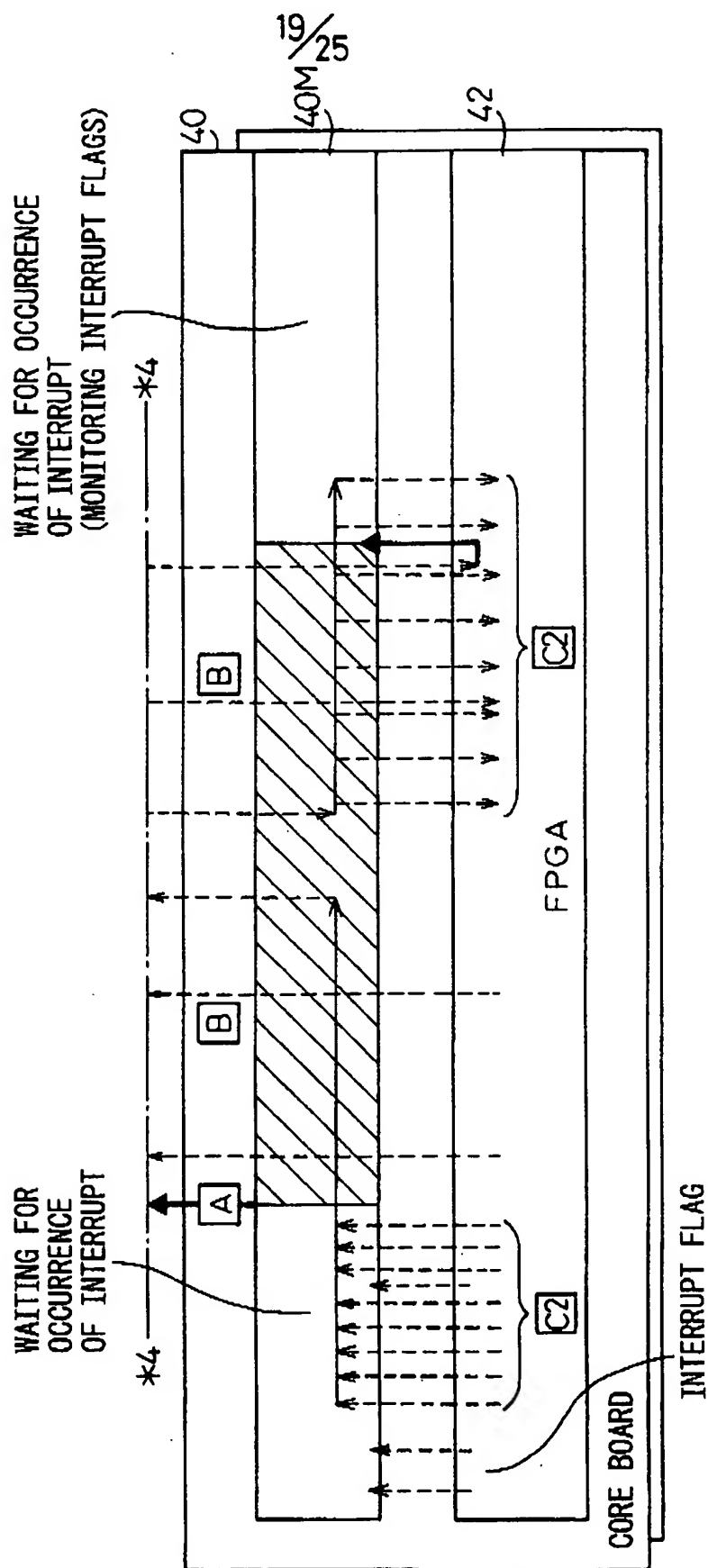
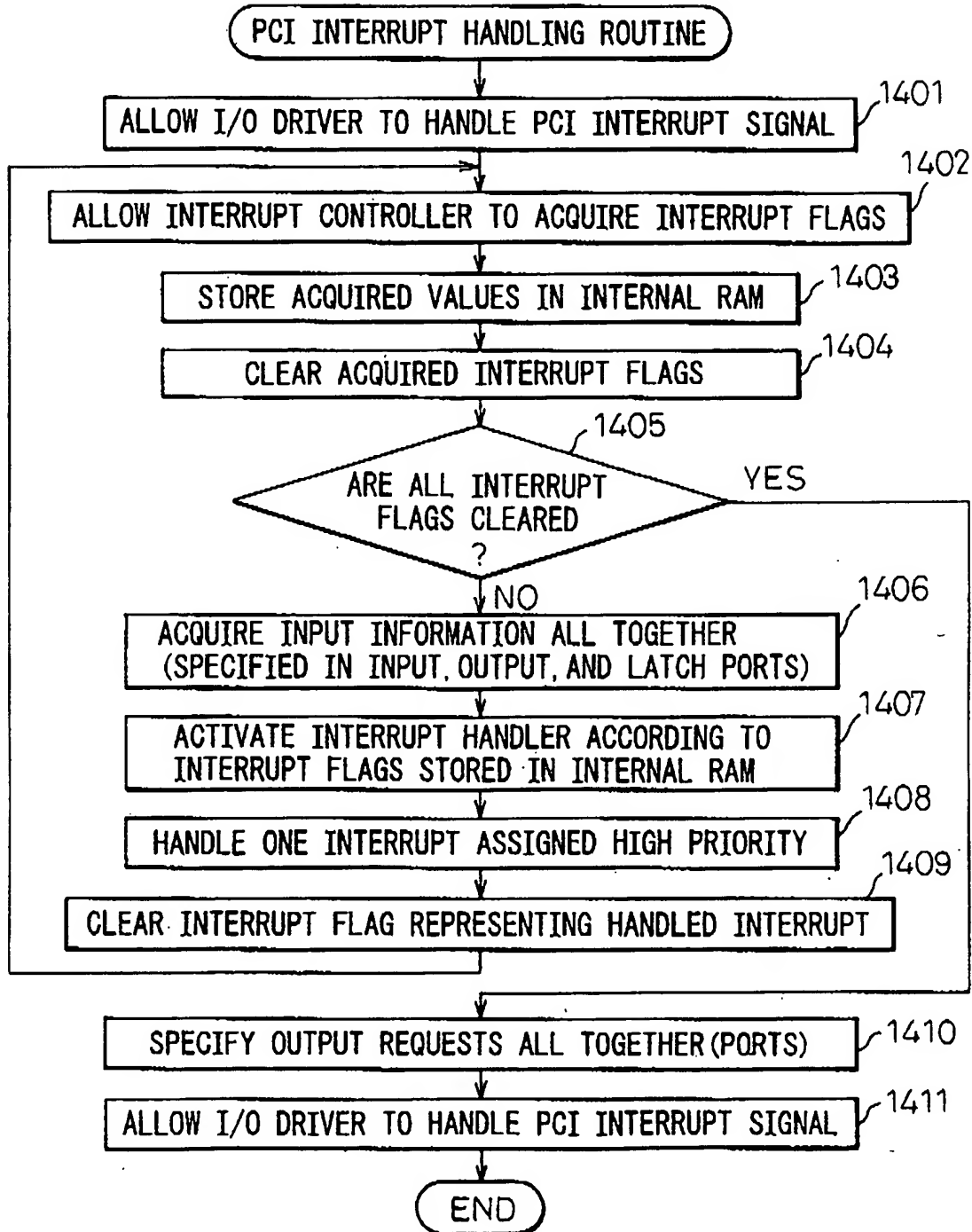


Fig. 13B



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Fig.14



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Fig.15

(a)

.....	CH5	CH4	CH3	CH2	CH1	CH0
.....	0	0	1	0	0	1

READ 1 AS PRESENCE OF AN INTERRUPT FACTOR,  
AND READ 0 AS ABSENCE OF AN INTERRUPT FACTOR.  
WRITE 1 TO CLEAR DATA, AND WRITE 0 TO PRESERVE DATA.

(b)

CAPTURED VALUE ON CHANNEL CH0	
CAPTURED VALUE ON CHANNEL CH1	
CAPTURED VALUE ON CHANNEL CH2	
CAPTURED VALUE ON CHANNEL CH3	
CAPTURED VALUE ON CHANNEL CH4	
CAPTURED VALUE ON CHANNEL CH5	
32 BITS IN WIDTH	

Fig. 16

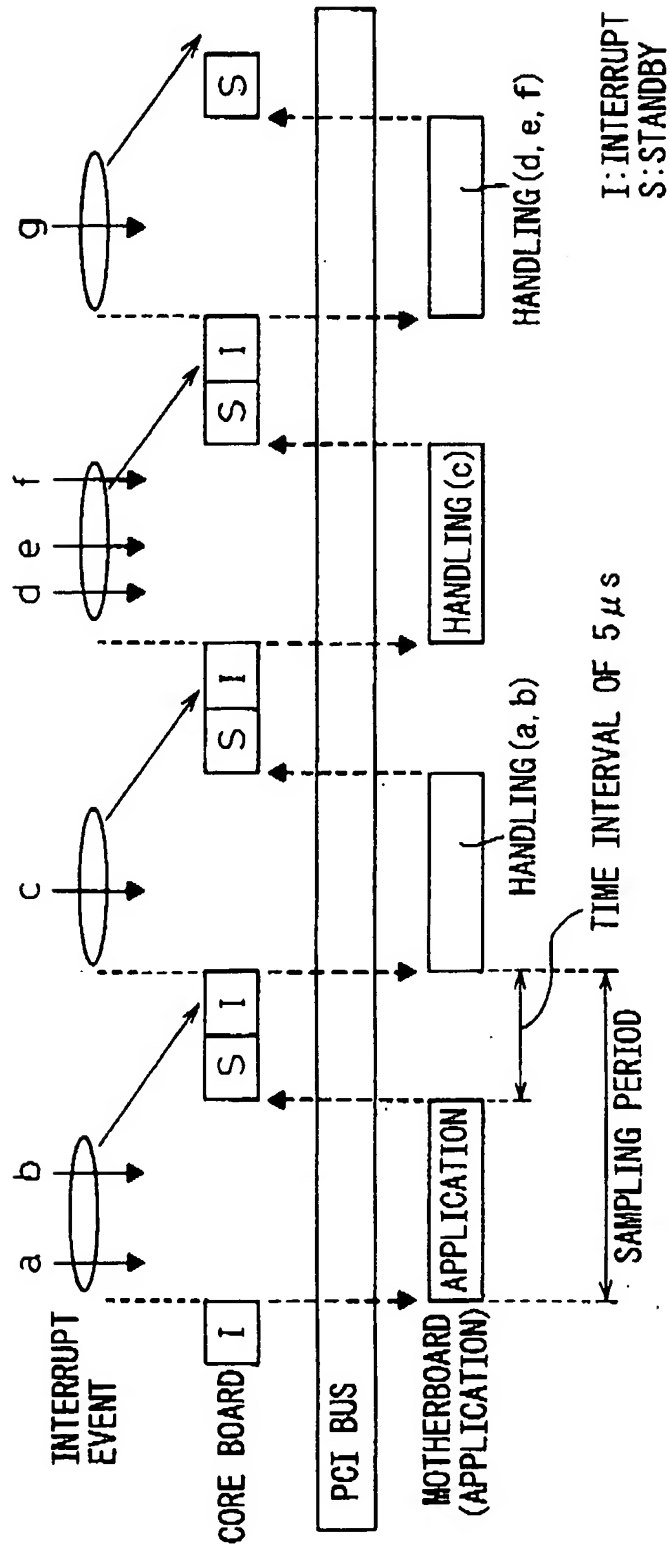
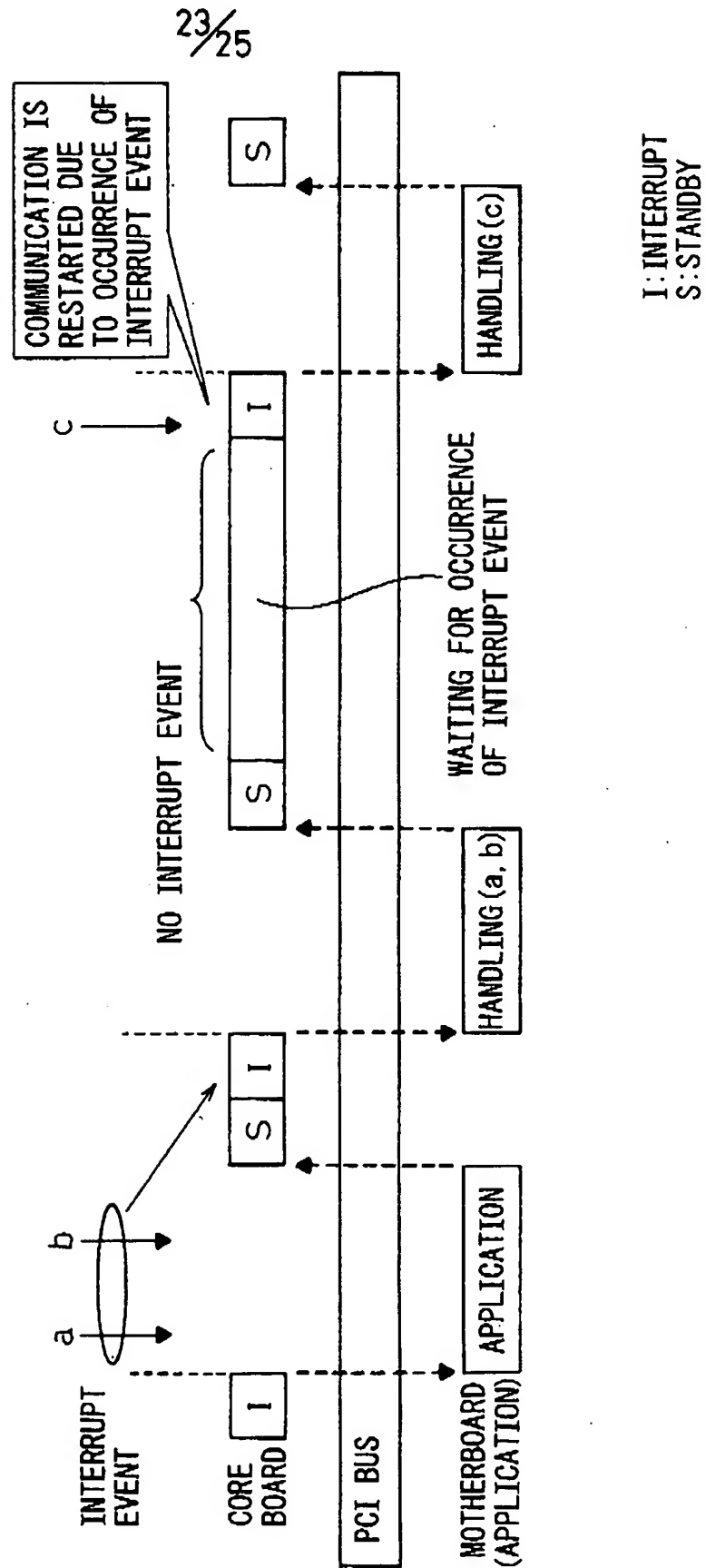
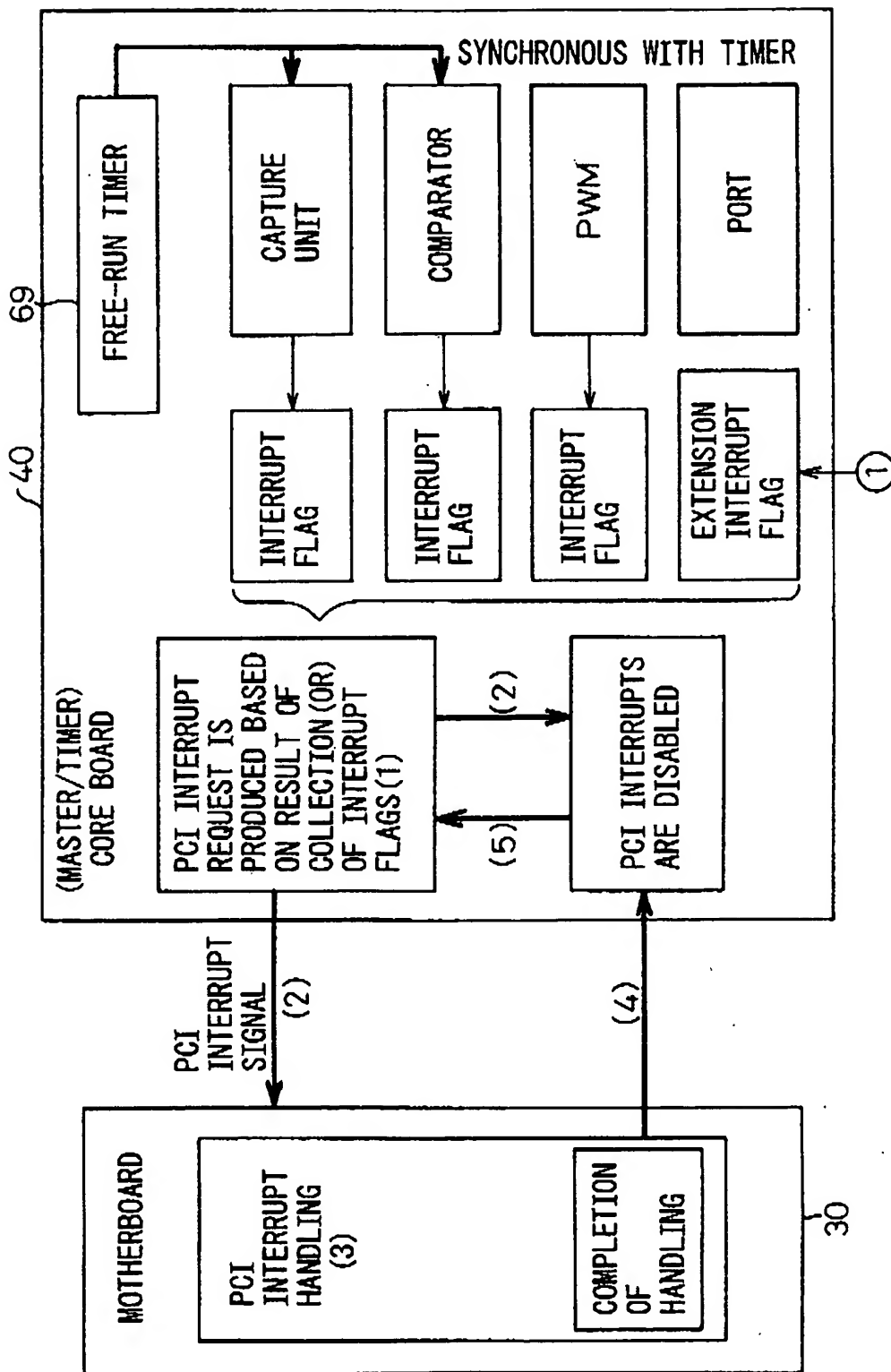


Fig.17



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Fig.18A





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Fig.18B

